

Customer No.: 31561
Application No.: 10/604,692
Docket No.: 10156-US-PA

REMARKS

Present Status of the Application

Under 35 U.S.C. 103(a), claims 1, 4-6, 8-10 and 35-37 were rejected as unpatentable over Kamigaki (US 6,894,344) in view of Lee (US 6,862,223), and claims 11-12 rejected as being unpatentable over Kamigaki in view of Lee and Schwabe (US 4,257,832).

In response, Applicants further amended independent claims 1 and 35 and submitted the following remarks, wherein the amendment is supported by, for example, [0018] and FIG. 1. Reconsideration of claims 1, 4-6, 8-12 and 35-37 is respectfully requested.

Discussion of Rejections under 35 U.S.C. 103(a)

One feature of amended independent claims 1 and 35 is that any two neighboring conductive pieces have two opposite edge portions over the charge-trapping layer that together cause a locally stronger electric field in operation of the memory cell such that only one coding region is defined, by the two neighboring conductive pieces, in the charge-trapping layer around the two opposite edge portions.

Kamigaki fails to disclose, teach or imply the above feature. Though the two shorted neighboring conductive pieces 7-1 do have two opposite edge portions over the charge-trapping layer "2-1+2-2", the two opposite edge portions of 7-1 are too distant from each other to together cause a locally stronger electric field. Moreover, as shown in col. 26, line 52, the charge-trapping layer "2-1+2-2" is called [two] store areas and the two store areas 2-1 and 2-2 are written independently *as controlled by the direction of the channel*

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current (see FIG. 2). Hence, there are two coding regions defined by the two neighboring conductive pieces 7-1, and the two coding regions are not defined by a locally stronger electric field caused by the two opposite edge portions of the two pieces 7-1.

Lee also fails to disclose, teach or imply the above feature of amended claim 1/35. Though the two shorted neighboring conductive pieces of SG1 or SG2 do have two opposite edge portions, the two conductive pieces form a select gate not for charge trapping (charges are stored in the FG) and the two opposite edge portions thereof are over no charge-trapping layer and define no coding region.

Moreover, it is quite non-obvious to combine Kamigaki and Lee to obtain the above feature of amended claim 1/35, at least for i) the two conductive pieces 7-1 in Kamigaki are arranged *laterally* but those of SG1 or SG2 in Lee are stacked *vertically*, ii) the function of the conductive pieces 7-1 as two control gates in Kamigaki is quite different from that of a select gate SG1 or SG2 in Lee, and iii) the switch gate 6 in Kamigaki is an essential element of the memory cell structure according to any operating mechanism disclosed in Kamigaki.

It is also noted that Schwabe, which was cited for the material of the charge-trapping layer and the conductivity types of the substrate and source/drain, also fails to disclose, teach or imply the above feature of amended claim 1/35.

Accordingly, at least the above feature of amended claim 1/35 cannot be obtained by combining Kamigaki and Lee (+ Schwabe). Moreover, the operating method of amended claim 35 is quite different from and non-obvious over any combination of those described in the three references, for the memory cell structure in claim 35 is quite different from and non-obvious over any combination of those described in the three references.

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For at least the above reasons, Applicants respectfully submit that claims 1 & 35 and claims 4-6, 8-12 & 36-37 dependent therefrom all patently define over the prior art.

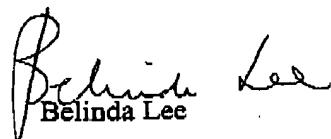
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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 4-6, 8- 12 and 35-37 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

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Respectfully submitted,


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